WHAT IS CLAIMED IS:

1. A contact for use in an integrated circuit, comprising:

a via located in a substrate; and

a contact plug located in said via, wherein said contact plug has a first portion having a notch removed therefrom and a second portion filling said notch.

2. The contact as recited in Claim 1 wherein said first and second portions comprise tungsten.

3. The contact as recited in Claim 1 wherein said notch has a depth ranging from about 20 nm to about 600 nm.

4. The contact as recited in Claim 1 wherein an opening of said notch has an width ranging from about 50 nm to about 150 nm.

5. The contact as recited in Claim 1 further including an adhesion layer located within said notch and between said first and second portions.

6. The contact as recited in Claim 5 wherein said adhesion layer has a thickness ranging from about 5 nm to about 15 nm.

7. The contact as recited in Claim 5 wherein said adhesion layer is a titanium/titanium nitride adhesion layer.

8. The contact as recited in Claim 1 being substantially free of a seam or void.

9. A method for manufacturing a contact for use in an integrated circuit, comprising:

forming a via in a substrate; and

placing a contact plug in said via, wherein said contact plug has a first portion having a notch removed therefrom and a second portion filling said notch.

10. The method as recited in Claim 9 wherein said placing includes etching said notch within said first portion and subsequently depositing said second portion within said notch.

11. The method as recited in Claim 9 wherein said placing a contact plug having first and second portions include placing a contact plug having first and second tungsten portions.

12. The method as recited in Claim 9 wherein said notch has a depth ranging from about 20 nm to about 600 nm.

13. The method as recited in Claim 9 wherein an opening of said notch has an width ranging from about 50 nm to about 150 nm.

14. The method as recited in Claim 9 further including depositing an adhesion layer within said notch and between said first portion and said second portion.

15. The method as recited in Claim 14 wherein depositing an adhesion layer includes depositing an adhesion layer having a thickness ranging from about 5 nm to about 15 nm.

16. The method as recited in Claim 14 wherein depositing an adhesion layer includes depositing a titanium/titanium nitride adhesion layer.

17. The method as recited in Claim 9 wherein said placing includes placing a contact plug in said via being substantially free of a seam or void.

18. An integrated circuit, comprising:

transistors located over a substrate; and

an interlevel dielectric layer located over said transistors, said interlevel dielectric layer having a contact for contacting said transistors located therein, said contact including;

a via located in said interlevel dielectric layer; and

a contact plug located in said via, wherein said contact plug has a first portion having a notch removed therefrom and a second portion filling said notch.

19. The integrated circuit as recited in Claim 18 further including an adhesion layer located within said notch and between said first portion and said second portion.

20. The integrated circuit as recited in Claim 18 wherein said transistors are selected from the group consisting of:

CMOS devices;

BiCMOS devices; and

bipolar devices.